

Circuit Description (continued)

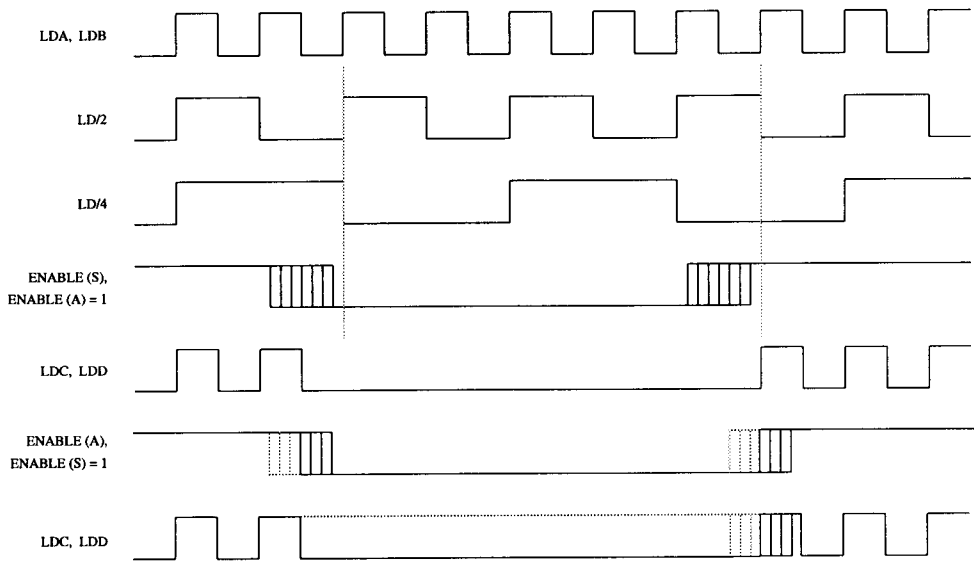


Figure 2. Load Output Timing.

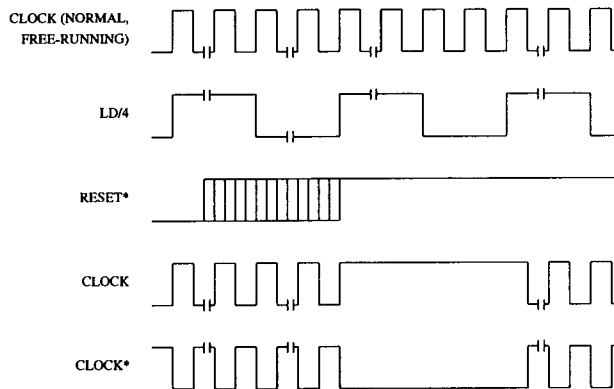


Figure 3. RESET* Timing.

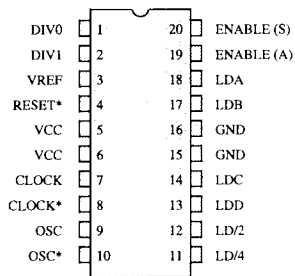
Pin Descriptions

| Pin Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|---|-----------------|------------------|-------------------|------------------|-------------------|---|---|----|---|---|---|---|----|---|---|---|---|----|---|---|---|---|----|---|---|
| VREF | Voltage reference output. This output provides a 1.2 V (typical) reference and may be used to drive the VREF input of up to four RAMDACs. | | | | | | | | | | | | | | | | | | | | | | | | | |
| OSC, OSC* | Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5 V supply. | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLOCK, CLOCK* | Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and these outputs can drive up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply. | | | | | | | | | | | | | | | | | | | | | | | | | |
| DIV0, DIV1 | Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified below: <table border="1" data-bbox="454 659 1075 855"> <thead> <tr> <th>DIV1</th> <th>DIV0</th> <th>Division Factor</th> <th>Clock Cycles Low</th> <th>Clock Cycles High</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>+3</td> <td>1</td> <td>2</td> </tr> <tr> <td>0</td> <td>1</td> <td>+4</td> <td>2</td> <td>2</td> </tr> <tr> <td>1</td> <td>0</td> <td>+5</td> <td>2</td> <td>3</td> </tr> <tr> <td>1</td> <td>1</td> <td>+8</td> <td>4</td> <td>4</td> </tr> </tbody> </table> | DIV1 | DIV0 | Division Factor | Clock Cycles Low | Clock Cycles High | 0 | 0 | +3 | 1 | 2 | 0 | 1 | +4 | 2 | 2 | 1 | 0 | +5 | 2 | 3 | 1 | 1 | +8 | 4 | 4 |
| DIV1 | DIV0 | Division Factor | Clock Cycles Low | Clock Cycles High | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | +3 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | +4 | 2 | 2 | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | +5 | 2 | 3 | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | +8 | 4 | 4 | | | | | | | | | | | | | | | | | | | | | | |
| LDA, LDB | Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by 3, 4, 5, or 8, as determined by the DIV0 and DIV1 inputs. | | | | | | | | | | | | | | | | | | | | | | | | | |
| LD/2 | Load output (TTL compatible). LD/2 is generated by dividing LDA by 2. | | | | | | | | | | | | | | | | | | | | | | | | | |
| LD/4 | Load output (TTL compatible). LD/4 is generated by dividing LDA by 4. | | | | | | | | | | | | | | | | | | | | | | | | | |
| LDC, LDD | Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs. | | | | | | | | | | | | | | | | | | | | | | | | | |
| ENABLE (S) | Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA, and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be logical zeros. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free-running and in phase with the LDA and LDB outputs. | | | | | | | | | | | | | | | | | | | | | | | | | |
| ENABLE (A) | Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were in when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are logical ones, LDC and LDD are free running and in phase with the LDA and LDB outputs. Glitches should be avoided on this asynchronous input. | | | | | | | | | | | | | | | | | | | | | | | | | |

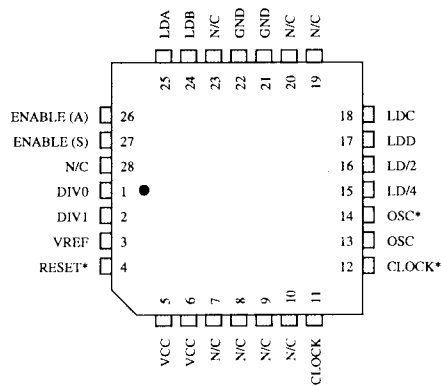
Pin Descriptions (continued)

| Pin Name | Description |
|----------|--|
| RESET* | Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free running. Glitches should be avoided on this edge-triggered input. |
| VCC | Device power. All VCC pins must be connected. |
| GND | Device ground. All GND pins must be connected. |

A 20-pin DIP Package



A 28-pin Plastic J-Lead (PLCC) Package



Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to a RAMDAC when using a differential ECL oscillator. The Bt438 should be located as close as possible to the RAMDAC. The 220 Ω resistors at the oscillator should be located as close as possible to the OSC and OSC* outputs. The 150 Ω resistor at the Bt438 should be located as close as possible to the Bt438 OSC and OSC* inputs.

The 220 Ω resistors at the Bt438 should be located as close as possible to the Bt438 CLOCK and CLOCK* outputs. The 150 Ω resistor at the RAMDAC should be located as close as possible to the CLOCK and CLOCK* inputs.

Figure 5 illustrates interfacing to a single-ended ECL oscillator.

Figure 6 shows interfacing to a TTL clock for applications less than 80 MHz. The +5 V of the resistor divider should be tied directly to the device +5 V. At VCC max, noise margin is at the minimum (100 mV).

Because of the inability to ensure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

A 1 kΩ resistor must be used to isolate the VREF output between multiple RAMDACs. This keeps noise on the Bt438 voltage reference from being coupled into the RAMDAC's VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA or GND, as specified in the RAMDAC's datasheet.

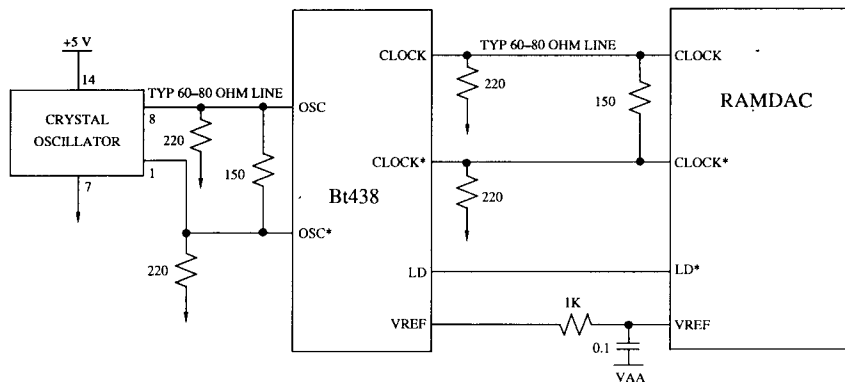


Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)

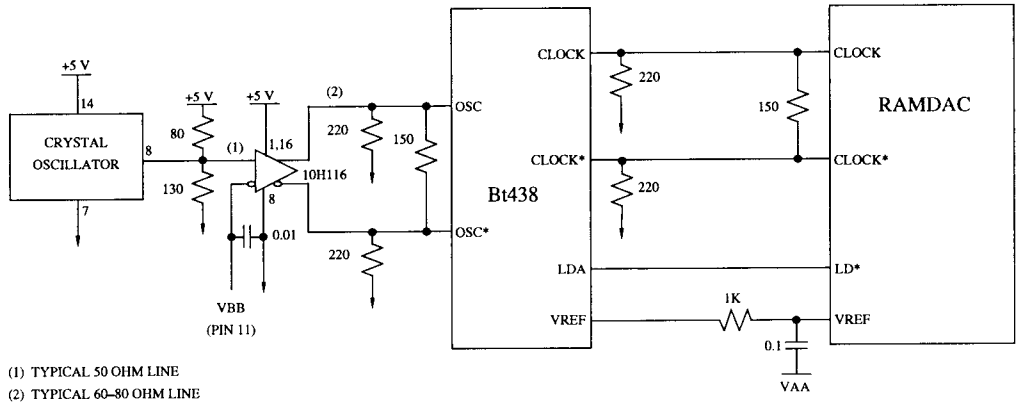


Figure 5. Interfacing to a Single-Ended Crystal Oscillator.

7

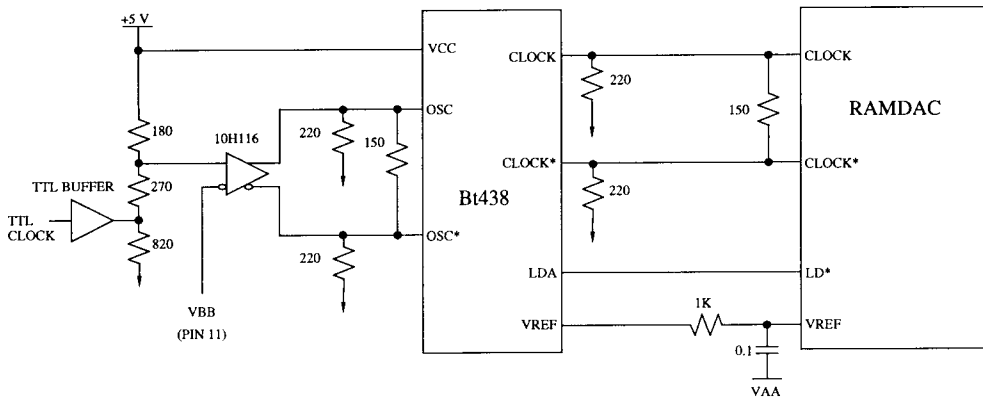


Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|-------------------------------|--------|------|------|------|-------|
| Power Supply | VCC | 4.75 | 5.00 | 5.25 | V |
| Ambient Operating Temperature | TA | 0 | | +70 | °C |
| OSC/OSC* Duty Cycle | | 40 | | | % |

Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|---|--------|---------|-----|-----------|----------|
| VCC (measured to GND) | | | | 7.0 | V |
| Voltage on any Pin | | GND-0.5 | | VCC + 0.5 | V |
| CLOCK, CLOCK* Output Current | | | | 30 | mA |
| Ambient Operating Temperature | TA | -55 | | +125 | °C |
| Storage Temperature | TS | -65 | | +150 | °C |
| Junction Temperature | TJ | | | | |
| Ceramic Package | | | | +175 | °C |
| Plastic Package | | | | +150 | °C |
| Soldering Temperature (5 seconds, 1/4" from pin) | TSOL | | | 260 | °C |
| Vapor Phase Soldering (1 minute) | TVSOL | | | 220 | °C |
| Air Flow | | 0 | | | l.f.p.m. |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

| Parameter | Symbol | Min | Typ | Max | Units |
|---|--------|---------|-----|-----------|-------|
| TTL Inputs | | | | | |
| Input High Voltage (general) | VIH | 2.0 | | VCC + 0.5 | V |
| DIV0, DIV1 | | 2.2 | | VCC + 0.5 | V |
| RESET* (at 0 °C) | | 2.2 | | VCC + 0.5 | V |
| Input Low Voltage | VIL | GND–0.5 | | 0.8 | V |
| Input High Current (Vin = 2.4 V) | IIH | | | 10 | µA |
| Input Low Current (Vin = 0.4 V) | IIL | | | –0.7 | mA |
| Input Capacitance (f = 1 MHz, Vin = 2.4 V) | CIN | | 4 | | pF |
| ECL Inputs | | | | | |
| Input High Voltage | VIH | VCC–1.1 | | VCC–0.8 | V |
| Input Low Voltage | VIL | GND–0.5 | | VCC–1.5 | V |
| Input High Current (Vin = 4.0 V) | IIH | | | 15 | µA |
| Input Low Current (Vin = 0.4 V) | IIL | | | 15 | µA |
| Input Capacitance (f = 1 MHz, Vin = 4.0 V) | CIN | | 4 | | pF |
| Load Outputs | | | | | |
| Output High Voltage (IOH = –2 mA) | VOH | 2.4 | | | V |
| Output Low Voltage (IOL = 20 mA) | VOL | | | 0.65 | V |
| Output Capacitance | | | 10 | | pF |
| Clock Outputs | | | | | |
| Differential Output Voltage | ΔVOUT | 0.6 | | | V |
| Output Capacitance | COUT | | 7 | | pF |
| Voltage Reference | | | | | |
| Output Voltage (Bt438 Rev. C) (Note 1) | VREF | 1.12 | 1.2 | 1.27 | V |
| Output Current | IREF | | 100 | | µA |
| VCC Supply Current (Note 2) | ICC | | 65 | 85 | mA |

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: RSET of the RAMDAC should be adjusted because the output voltage of the Bt438 Rev. C is lower than the recommended VREF for the RAMDAC. $I_{OG} \text{ (mA)} = \frac{11294 \cdot V_{REF}}{R_{SET}}$, $I_{OG} \text{ (typ)} = 26.7 \text{ mA}$.

Note 2: Measured without 50 Ω to VCC–2 V on CLOCK and CLOCK*.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------------------|--------|------|-----|-----|-------|
| OSC, OSC* Clock Rate | Fmax | | | 250 | MHz |
| LDA Output Delay (Note 1) | 1 | | 4 | 10 | ns |
| LDA, LDB Pulse Width Low (Note 2) | | 5 | | | ns |
| LDA to LDB Output Skew (Note 3) | | -2.0 | 0 | 2.0 | ns |
| LDA to LDC Output Skew (Note 3) | | -1.0 | 1.5 | 4.0 | ns |
| LDA to LD/2 Output Skew (Note 3) | | 0 | 1.5 | 5.0 | ns |
| LDA to LD/4 Output Skew (Note 3) | | 0 | 1.5 | 6.0 | ns |
| LDC to LDD Output Skew (Note 3) | | -2.0 | 0 | 2.0 | ns |
| RESET* Active Low Time | 2 | 15 | | | ns |
| RESET* Setup Time | 3 | 12 | | | ns |
| ENABLE (S) Setup Time | 4 | 12 | | | ns |
| ENABLE (S) Hold Time | 5 | -2 | | | ns |
| ENABLE (A) Setup Time | 6 | 12 | | | ns |
| ENABLE (A) Hold Time | 7 | -2 | | | ns |

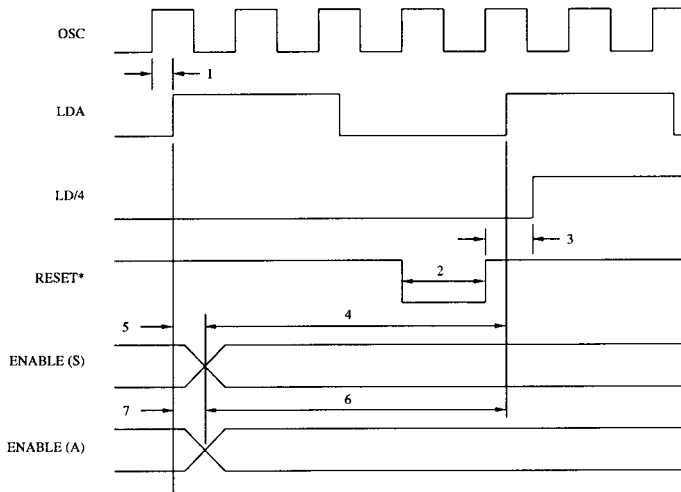
Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 Ω to VCC-2 V. TTL outputs have -2 mA/20 mA load applied with 1.5 V switching point. TTL input values are 0-3 V with input rise/fall times \leq 4 ns, measured between 10-percent and 90-percent points. ECL input values are VCC-1.8 to VCC-0.8 V with input rise/fall times \leq 1 ns, measured between 20-percent and 80-percent points. Timing reference points at 50-percent for inputs and outputs, except TTL outputs measured at 1.5 V. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: Output load = 50 pF.

Note 2: LD outputs not used in +3 over 200 MHz.

Note 3: LD outputs equally loaded. Unequal loading may result in additional output skew.

Timing Waveforms



Input/Output Timing

Ordering Information

| Model Number | Package | Ambient Temperature Range |
|--------------|-----------------------|---------------------------|
| Bt438KC | 20-pin 0.3" Cerdip | 0° to +70° C |
| Bt438KPJ | 28-pin Plastic J-Lead | 0° to +70° C |